A Theory of Distributed Amplifiers Exploiting Growing Waves

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ABSTRACT

Providing a discussion of the basic mechanisms of mode coupling and positive feed-back along FET electrodes, we propose some possible applications of the growing waves phenomena to distributed (continuous and discrete) amplifier design.

INTRODUCTION

Distributed amplification can be theoretically obtained in two different ways [1]:

1- By using the chain amplifier concept, namely the DA (distributed amplification) operation, in which a device operates as many parallel devices, distributed along two lines: in this category can be included the configuration proposed by McIver in [2]; gain is linearly dependent on the device length.

2- By using the growing-wave concept (GW): if a distributed structure supports a growing mode, exciting this mode gives rise to a symmetric active device similar to an optical amplifier; gain is exponentially dependent on the device length.

Khon and Landauer [3] first showed that this phenomenon may take place if a feed-back parasitic capacitance is included in McIver's device. Whereas a large number of works on the subject followed [3], a systematic description of the parameters controlling such phenomena escaped investigation.

This paper addresses the kind of operation described under 2: providing an explanation of the basic coupling and feed-back mechanism giving rise to growing modes, we point out some basic rules of the GW amplifier design. As validation, such rules are successfully used to design some distributed GW discrete amplifiers.

MODELLING

In this paper we made use of a distributed equivalent-circuit model: the active device is represented by three coupled lines (see fig.1); starting from Kirchoff laws, the transmission line equations are obtained in matrix form. Such equations are manipulated in order to get an eigenvalue equation whose solution provide the modal voltage and current distribution (see e.g. [7]).

THEORY AND CLASSIFICATION

The different coupling phenomena and the resulting effects on the device modes were independently considered.

- Let us consider three uncoupled lossless lines. Introducing a passive capacitive coupling (C_{dg} ,C_{gs} and C_{ds}), two new modes appear: the eigenvectors are reported in fig. 2 for the special case of a symmetrical structure. In this latter instance, accordingly to the definition of fig.2, the bulk mode is the fastest mode and is insensitive to coupling, whereas the gate (even) mode is the slowest one. A third mode exists having an intermediate velocity: the drain (odd) mode.
- Setting now $g_m \neq 0$, both the bulk and the drain (fast) mode become lossy, whereas the gate (slow) mode *grows exponentially.*
- By introducing $R_i = 0$, we get a first likely FET model with floating source. In

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order to recover the previous classification, the distributed circuit is made electrically symmetric, by setting the parallel combination of C_g and C_{gs} equal to C_{ds}. In this case the drain mode becomes very lossy, whereas gate and bulk mode do not interact with the channel current: the drain mode gate-source and drain-source voltages are both in phase with the channel current, so that the inner product between the electric field **E** and the channel current **J** is greater than zero and the wave, accordingly to Poynting's theorem, loses power; for the gate mode, this product is positive in the gate-source part of the channel and negative in the gate-drain part, giving no global interaction [6]. As to the bulk mode, **E** and **J**, being orthogonal do not exchange power.

- Let us alter C_{gs} and C_{dg}. Accordingly to our speed-dependent mode definition, by raising C_{gs} and reducing C_{gd} for zero transconductance, the bulk (and the drain) mode fields tend to redistribute near the gate-to-drain gap, charging C_{gd}, whereas the gate mode field distribution approaches a relative maximum between the gate and source electrodes. On the other hand, by raising C_{gd} and reducing C_{gs}, the bulk and gate modes behave dually.

These considerations allow to explain the behaviors of fig.3, obtained when $g_m \neq 0$, by means of the Poynting's theorem: whereas the drain mode is still lossy and, due to the direction of the gate-to-drain voltage, losses are monotonically raised with C_{gd}, the bulk mode is lossy for $C_{gs}<C_{gd}$, lossless for $C_{gs}=C_{gd}$ and *growing* for $C_{gs}>C_{gd}$. The gate mode, on the other hand, behaves "dually".

- Introducing the capacitance C_{ds} in a symmetric structure, owing to their symmetry, the bulk and gate mode are unaffected. The drain mode losses, instead, tend to be *asymptotically* compensated by the insertion of such a capacitance (fig. 4a): C_{ds} closes an "external" parasitic circuit to the controlled source g_m, and the injected current has now the right phase relationship with the modal voltages, in order to gain energy. The introduction of the overlay capacitance C_{ds} in an asymmetric structure having $C_{gs}> C_{gd}$, could then give rise to a *growing drain mode*, as shown in fig.4b, the lossy interaction being minimum (fig.3).

- Let us now consider the starting situation of three lines without either transconductive or capacitive coupling. Introducing a mutual inductive coupling (L_{dg}, L_{gs} and L_{ds}) again three different modes appear, but now the *slowest mode is the "bulk"-mode*, as defined by the voltage distribution of fig 2; the fastest one is the gate-mode whereas the drain-mode is also a fast wave. It is now clear that for $g_m \neq 0$, in the symmetric case (L_{dg}, L_{gs}), the *fastest mode grows.* This is because the fastest mode now assumes the voltage distribution of the gate mode whereas the slow mode is lossy. More generally, a *duality property holds* in the other cases considered above.

The two kinds of bilateral couplings (capacitive and inductive) are then mutually *conflicting.*

APPLICATIONS: DISTRIBUTED DISCRETE GW-AMPLIFIERs

The principles introduced in the previous section may be used in order to design a distributed continuous GW-TWFET such as the ones proposed in [4], in [5] or in [6], but we tried to check the theory by making recourse to discrete chain amplifiers to overcome some practical difficulties.

In order to realize a discrete ladder network equivalent to a distributed circuit, voltages and currents ought not to vary too fast from one stage to another, i.e. for the excited mode must be $\beta < 2\pi$. To this aim a *fast* (growing) wave is suitable and, in view

of higher efficiency, we selected a "drain" mode, accordingly to the definitions introduced in the previous section: the necessary condition to be satisfied is then $C_{gs}>C_{gd}$, with a capacitance C_{ds} of the same order of magnitude as C_{gs}.

We have developed an example of low frequency amplifier: for a low frequency n-channel FET BF245B we get, by biasing in the saturation region (Vgs=0V, Vds=3V) a transconductance as high as g_m=7.1 mS. An equivalent "distributed" transistor constituted by 10 FETs will have g_m=71 mS for unit length. Propagation and attenuation constants in the frequency range from 1 to 10 MHz are reported in fig. 5. As to the terminations, the device is fed at the gate electrode whereas the remaining electrodes is terminated on "hidden" loads, these being assumed approximately equal to the characteristic impedance computed for the growing mode at the source and drain lines, respectively (fig 6). The knowledge of the eigenvectors (according to discussion of sec. II) allows to compute the reduced Z-matrix representing the two-port circuit accessible at the gate line: the optimum termination is then obtained from circuit theory, stating that the load impedance ought to be the device image impedance.

The simulated S-parameters are reported in fig. 7, showing that, in spite of the simplicity of the above design considerations, the resulting device shows gain.

To check the idea on the discrete circuit, a discrete ladder network is arranged accordingly to fig. 8. Fig. 9 depicts the results computed by the Spice circuit simulation tool: a complete agreement between the distributed and the discrete circuits is obtained in the frequency range where the inequality $\beta < 2\pi$ is strictly satisfied for each mode (see fig. 5).

The maximum observed gain is 5dB at about 4.5 MHz. As not only the growing mode is excited, higher gains are easily obtained by suitably changing the termination ports (e.g. terminating to 560Ω the drain and source port and to 390 Ω the gate port gives rise to a gain of about 10dB); obviously one pays for this improvement by greater potential instability.

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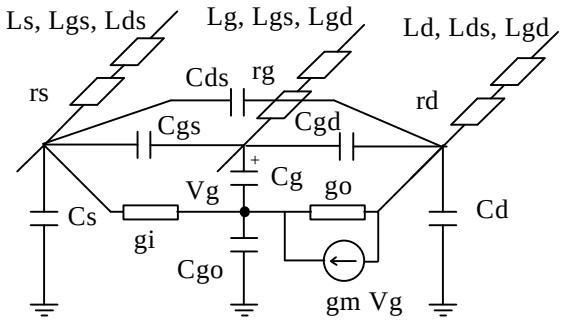


Fig.1: Three line circuit model

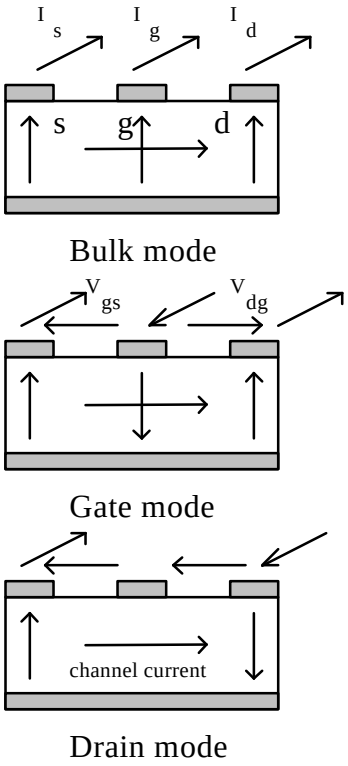


Fig. 2: modal voltages and currents for three identical lines.

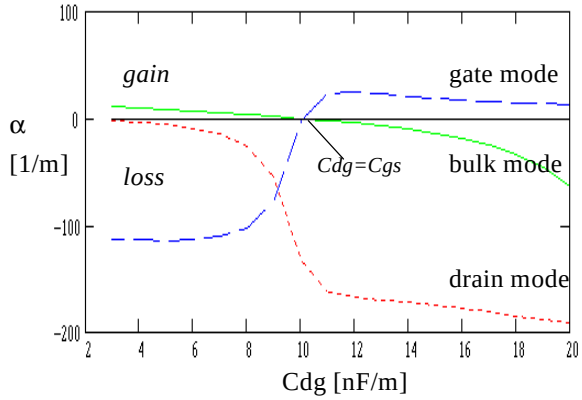


Fig. 3: attenuation constant versus feed-back capacitance (floating source model): Cdg+Cgs=20 nF/m; f= 1 GHz, Ri=0, gm=10 mS/mm, ld=ls=14.6 µH/m, lg=2.9 µH/m, Cd=Cs= 1nF/m; the other parameters are assumed negligible;

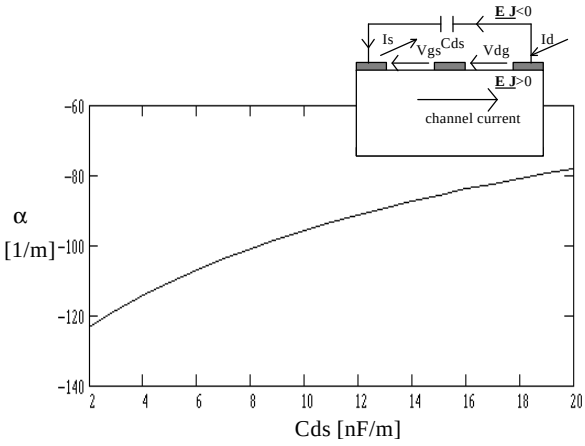
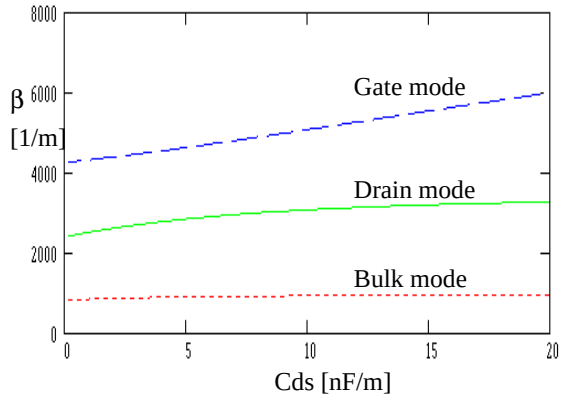


Fig. 4a: propagation and attenuation constant versus capacitance Cds in a symmetric structure (floating source model): the drain mode losses appear to be asymptotically reduced by the insertion of Cds. Cgs=Cgd=10 nF/m. For the other parameters see fig.3



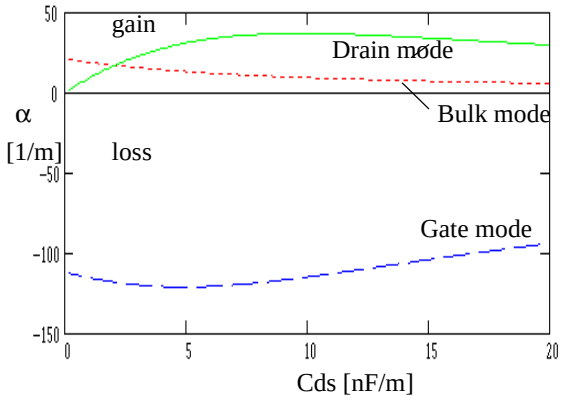
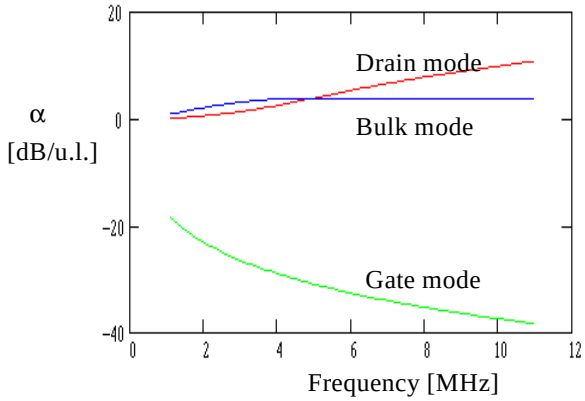


Fig. 4b: attenuation and propagation constants versus capacitance Cds in an asymmetric structure (floating source model). Cgs=19 nF/m, Cgd= 1 nF/m.



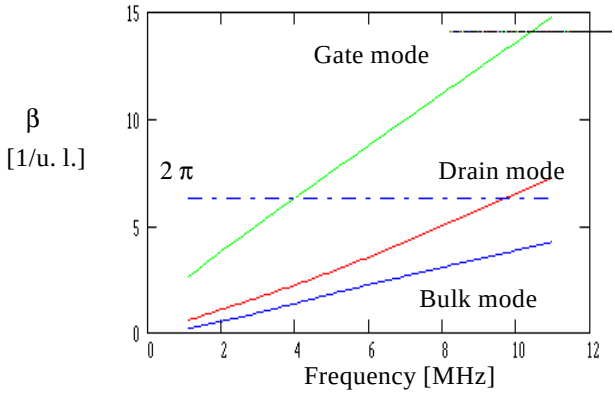


Fig. 5: attenuation and propagation constants of the distributed network; the network parameters are Ld=Lg=Ls=22μH/u.l., Cd=Cs= 330pF/u.l., Cg=470 pF/u.l., Cds=470pF/u.l., Cgd=10pF/u.l., go= 256μS/u.l., g_m= 71mS/u.l.; the remaining parameters are set equal to zero.

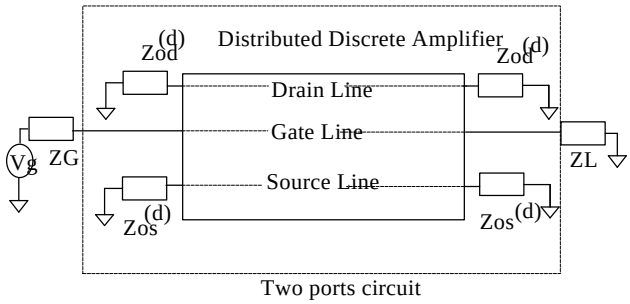


Fig. 6: a possible termination topology; note that $Zos^{(d)}$ stands for the characteristic impedance of the drain mode at the source port and $Zod^{(d)}$ is the same at the drain port

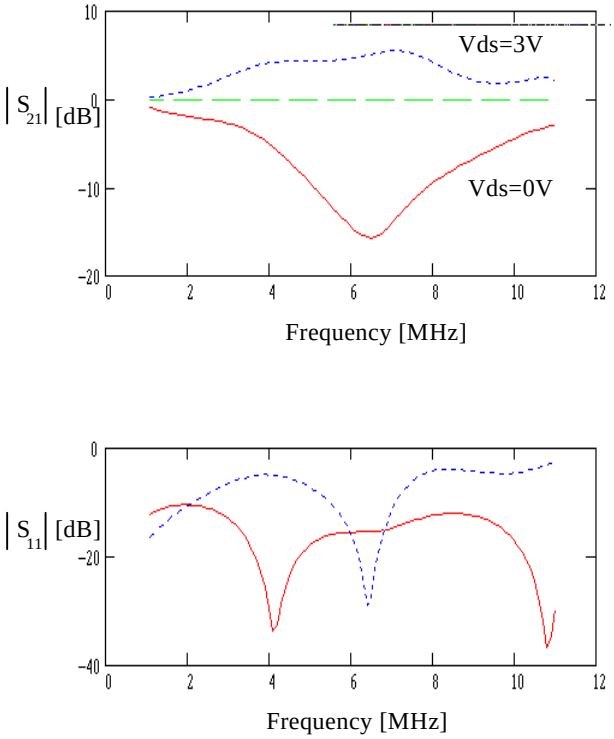


Fig. 7: S-parameters for the analysed device with $Zos^{(d)}$=$Zod^{(d)}$= 220Ω and ZL=ZG=330Ω.

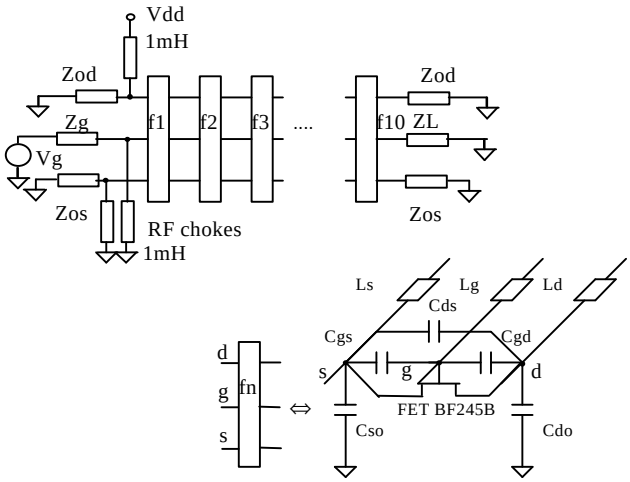


Fig. 8: the discrete ladder network: details and biasing.

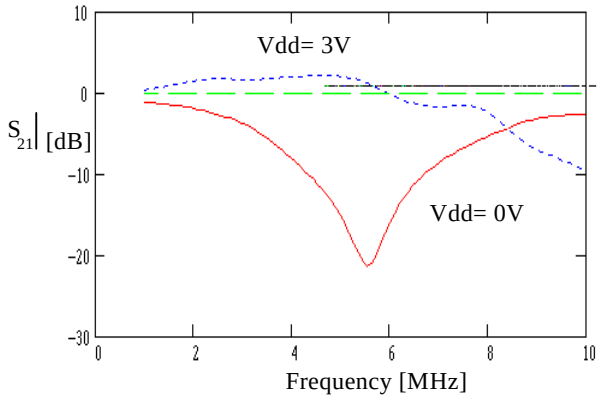


Fig. 9: Spice simulation of the discrete ladder network: Gain.